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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,123	SANDHU ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46,47 and 57-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *83 and 84* is/are allowed.

6)☒ Claim(s) *46,47,57-60,62-64,66-68,70-72,74-77 and 79-81* is/are rejected.

7)☒ Claim(s) *61,65,69,73 and 78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *June 25, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement filed June 25, 2004. A signed copy of Form PTO-1449 is herewith enclosed.

Response to Amendment

Amendment filed June 25, 2004 forms the basis of this official action. In said Amendment Applicant substantially amended claims 57-59 and added new claims 83-84.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 46*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al in view of Anjum et al (5,4501,674) (see Information Disclosure Statement filed June 25, 2004).

Nakamura et al teach a memory (device) (cf. title, abstract and col. 1, l. 5-10) comprising: a memory array (cf. Figure 1 and col. 4, l. 8-35 and col. 13, l. 49-58); a control circuit (the word driver of Figure 8, col. 14, l. 66 – col. 15, l. 7 and col. 15, l. 59-67), operatively coupled to the memory array (the word driver inherently drives the gates of the memory array); and an I/O circuit (input DIN / output buffer united into one

input/output buffer) (cf. col. 8, l. 24-37), operatively coupled to the memory array (inherently so, because said input/output buffer belong to the peripheral circuits of the memory array and have the function to provide input and output functions for said memory array; and wherein the memory array, control circuit and I/O circuit each comprise a MOSFET (see col. 8, l. 53-58 for the MOSFETS in the memory array, col. 15, l. 59-67 for the MOSFETs in the control circuit, and Figure 9 and col. 15, l. 42-48 for the MOSFETs in the I/O circuit).

Nakamura et al do not necessarily teach the limitation that each of said MOSFETs to comprise the claimed titanium alloy layer and titanium silicide contact of claim 46, which limitation when included would imply the teaching of the invention defined by claim 46.

However, it would have been obvious to include said limitation in view of Anjum et al: Anjum et al teach MISFET devices (cf. Figure 4, col. 5, l. 6-60) comprising: a layer of titanium alloy 40 (cf. col. 6, l. 34-47), wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic, and antimony, in particular: germanium; and a titanium silicide contact 38 (cf. col. 6, l. 34-47) having a composition different from the layer of titanium alloy (inherently the compositions of titanium silicide and titanium germanide are different), the contact being directly coupled to the layer (cf. Figure 7 and col. 6, l. 34-48; note that the titanium silicide is produced by an annealing step after the introduction of the germanium, and hence the silicide is in contact with the germanide).

The specific purpose is to reduce the required temperature for silicide formation and to reduce the thickness of the silicide layer, which if too thick would cause undue stresses in the layer (cf. col. 2, l. 25-42), in the formation of a barrier layer for the prevention of silicon migration into interconnect metal (cf. col. 1, l. 30-47). Said prevention is especially important for small-scale integrated circuits on a single chip (cf. col. 1, l. 13-30).

Motivation, to include the teaching by Anjun et al in the teaching by Nakamura et al is thus found in the objective by Nakamura on a memory device on a single chip (cf. col. 1, l. 5-10: integrated circuit) with increasingly fine element structures (cf. col. 2, l. 24-28) and the presence, in the invention by Nakamura et al of MOSFETs in all of the three cited components. The unspecified nature of the gate insulating film in the case of MISFETs as opposed to MOSFETs is irrelevant for this nexus. *Combination* of the teaching by Anjun et al in this regard and the invention by Nakamura et al is straightforward through the application to the source/drain contact structures in the MOSFETs by Nakamura et al of germanium to a titanium layer followed by annealing and removal of the upper portion of the titanium layer as disclosed by Anjun et al (cf. col. 6, l. 34-48). Success in implementing said combination can therefore be reasonably expected.

3. ***Claims 57 and 59*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al in view of Anjum et al (5,4501,674) (cf. IDS of June 25, 2004).

Nakamura et al teach a memory (device) (cf. title, abstract and col. 1, l. 5-10) comprising: a memory array (cf. Figure 1 and col. 4, l. 8-35 and col. 13, l. 49-58); a control circuit (the word driver of Figure 8, col. 14, l. 66 – col. 15, l. 7 and col. 15, l. 59-67), operatively coupled to the memory array (the word driver inherently drives the gates of the memory array); and an I/O circuit (input DIN / output buffer united into one input/output buffer) (cf. col. 8, l. 24-37), operatively coupled to the memory array (inherently so, because said input/output buffer belong to the peripheral circuits of the memory array and have the function to provide input and output functions for said memory array; and wherein *at least one* of the memory array, control circuit and I/O circuit comprise a MOSFET (see col. 8, l. 53-58 for the MOSFETS in the memory array, col. 15, l. 59-67 for the MOSFETs in the control circuit, and Figure 9 and col. 15, l. 42-48 for the MOSFETs in the I/O circuit).

Nakamura et al do not necessarily teach the limitation that each of said MOSFETs to comprise the claimed titanium alloy layer overlying walls of a contact hole and titanium silicide contact of claim 57, which limitation when included would be sufficient to imply the teaching of the invention defined by claim 57.

However, it would have been obvious to include said limitation in view of Anjum et al: Anjum et al teach MISFET devices (cf. Figure 4, col. 5, l. 6-60) comprising: a layer of titanium alloy 40 (cf. col. 6, l. 34-47) overlying the walls of a contact hole (i.e., the "contact window" of conductor 48 through dielectric layer 46 (cf. col. 6, l. 66 – col. 7, l. 9) , wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon,

germanium, lead, arsenic, and antimony, in particular: germanium; and a titanium silicide contact 38 (cf. col. 6, l. 34-47) having a composition different from the layer of titanium alloy (inherently the compositions of titanium silicide and titanium germanide are different), the contact being directly coupled to the layer (cf. Figure 7 and col. 6, l. 34-48; note that the titanium silicide is produced by an annealing step after the introduction of the germanium, and hence the silicide is in contact with the germanide).

The specific purpose is to reduce the required temperature for silicide formation and to reduce the thickness of the silicide layer, which if too thick would cause undue stresses in the layer (cf. col. 2, l. 25-42), in the formation of a barrier layer for the prevention of silicon migration into interconnect metal (cf. col. 1, l. 30-47). Said prevention is especially important for small-scale integrated circuits on a single chip (cf. col. 1, l. 13-30).

Motivation, to include the teaching by Anjun et al in the teaching by Nakamura et al is thus found in the objective by Nakamura on a memory device on a single chip (cf. col. 1, l. 5-10: integrated circuit) with increasingly fine element structures (cf. col. 2, l. 24-28) and the presence, in the invention by Nakamura et al of MOSFETs in all of the three cited components. The unspecified nature of the gate insulating film in the case of MISFETs as opposed to MOSFETs is irrelevant for this nexus. *Combination* of the teaching by Anjun et al in this regard and the invention by Nakamura et al is straightforward through the application to the source/drain contact structures in the MOSFETs by Nakamura et al of germanium to a titanium layer followed by annealing and removal of the upper portion of the titanium layer as disclosed by Anjun et al (cf.

col. 6, l. 34-48), while the interconnect structure including conductive layer 48 extending through dielectric layer 46 thus teaching the contact hole as taught by Anjum et al is an obvious aspect of a MOSFET. *Success* in implementing said combination can therefore be reasonably expected.

On claim 59: the text of the rejection of claim 57 is included herewith by reference for the rejection of all limitations included in lines 1-11 of claim 59, being identical to those of lines 1-11 of claim 57. Furthermore, the limitation "wherein the titanium alloy layer is produced using a method.....with the seed layer" is a limitation only on the method of making the device and thus fails to further limit the device invention as elected by original representation.

4. ***Claim 58*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al in view of Anjum et al (5,4501,674) (cf. IDS of June 25, 2004).

Nakamura et al teach a memory (device) (cf. title, abstract and col. 1, l. 5-10) comprising: a memory array (cf. Figure 1 and col. 4, l. 8-35 and col. 13, l. 49-58); a control circuit (the word driver of Figure 8, col. 14, l. 66 – col. 15, l. 7 and col. 15, l. 59-67), operatively coupled to the memory array (the word driver inherently drives the gates of the memory array); and an I/O circuit (input DIN / output buffer united into one input/output buffer) (cf. col. 8, l. 24-37), operatively coupled to the memory array (inherently so, because said input/output buffer belong to the peripheral circuits of the memory array and have the function to provide input and output functions for said memory array; and wherein *at least one* of the memory array, control circuit and I/O

circuit comprise a MOSFET (see col. 8, l. 53-58 for the MOSFETS in the memory array, col. 15, l. 59-67 for the MOSFETs in the control circuit, and Figure 9 and col. 15, l. 42-48 for the MOSFETs in the I/O circuit).

Nakamura et al do not necessarily teach the limitation that each of said MOSFETs to comprise the claimed via having titanium alloy layer overlying walls of a contact hole and titanium silicide contact of claim 58, which limitation when included would imply the teaching of the invention defined by claim 58.

However, it would have been obvious to include said limitation in view of Anjum et al: Anjum et al teach MISFET devices (cf. Figure 4, col. 5, l. 6-60) comprising a via (the via through dielectric layer 46 of conductive layer 48; cf. col. 6, l. 66 – col. 7, l. 9) having: a layer of titanium alloy 40 (cf. col. 6, l. 34-47) overlying the walls of a contact hole (i.e., the "contact window" of conductor 48 through dielectric layer 46 (cf. col. 6, l. 66 – col. 7, l. 9), wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, *germanium*, lead, arsenic, and antimony, in particular: *germanium*; and a titanium silicide contact 38 (cf. col. 6, l. 34-47) having a composition different from the layer of titanium alloy (inherently the compositions of titanium silicide and titanium germanide are different), the contact being directly coupled to the layer (cf. Figure 7 and col. 6, l. 34-48; note that the titanium silicide is produced by an annealing step after the introduction of the germanium, and hence the silicide is in contact with the germanide); and a fill 48 (cf. col. 7, l. 1) coupled to the titanium alloy layer (cf. col. 7, l. 6-9).

The specific purpose of this teaching by Anjum et al is to reduce the required temperature for silicide formation and to reduce the thickness of the silicide layer, which if too thick would cause undue stresses in the layer (cf. col. 2, l. 25-42), in the formation of a barrier layer for the prevention of silicon migration into interconnect metal (cf. col. 1, l. 30-47). Said prevention is especially important for small-scale integrated circuits on a single chip (cf. col. 1, l. 13-30).

Motivation, to include the teaching by Anjun et al in the teaching by Nakamura et al is thus found in the objective by Nakamura on a memory device on a single chip (cf. col. 1, l. 5-10: integrated circuit) with increasingly fine element structures (cf. col. 2, l. 24-28) and the presence, in the invention by Nakamura et al of MOSFETs in all of the three cited components. The unspecified nature of the gate insulating film in the case of MISFETs as opposed to MOSFETs is irrelevant for this nexus. *Combination* of the teaching by Anjun et al in this regard and the invention by Nakamura et al is straightforward through the application to the source/drain contact structures in the MOSFETs by Nakamura et al of germanium to a titanium layer followed by annealing and removal of the upper portion of the titanium layer as disclosed by Anjun et al (cf. col. 6, l. 34-48), while the interconnect structure including conductive layer 48 extending through dielectric layer 46 thus teaching the contact hole as taught by Anjum et al is an obvious aspect of a MOSFET. *Success* in implementing said combination can therefore be reasonably expected.

5. ***Claims 60 and 63*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al in view of Anjum et al (5,4501,674) (cf. IDS of June 25, 2004).

Nakamura et al teach a memory (device) (cf. title, abstract and col. 1, l. 5-10) comprising: a semiconductor substrate (cf. abstract, first sentence, and col. 3, l. 66 – col. 4, l. 8); a memory array (cf. Figure 1 and col. 4, l. 8-35 and col. 13, l. 49-58) coupled to the semiconductor substrate (cf. abstract, first sentence, and col. 4, l. 66 – col. 7, l. 8); a control circuit (the word driver of Figure 8, col. 14, l. 66 – col. 15, l. 7 and col. 15, l. 59-67), operatively coupled to the memory array (the word driver inherently drives the gates of the memory array); an I/O circuit (input DIN / output buffer united into one input/output buffer) (cf. col. 8, l. 24-37), operatively coupled to the memory array (inherently so, because said input/output buffer belong to the peripheral circuits of the memory array and have the function to provide input and output functions for said memory array); an electronic device (any of the MOSFETs in any of said memory array, control circuit or I/O circuit) (see col. 8, l. 53-58 for the MOSFETS in the memory array, col. 15, l. 59-67 for the MOSFETs in the control circuit, and Figure 9 and col. 15, l. 42-48 for the MOSFETs in the I/O circuit) coupled to the semiconductor substrate (inherent to a MOSFET is its coupling through a contact with a semiconductor substrate), the electronic device having an active region (inherent to any MOSFET) and an insulating layer over the active region (inherent in any MOSFET).

Nakamura et al do not necessarily teach the limitation that each of said MOSFETs to comprise the claimed alloy layer and titanium silicide layer defined by claim 60.

However, it would have been obvious to include said limitation in view of Anjum et al: Anjum et al teach MISFET devices (cf. Figure 4, col. 5, l. 6-60) comprising: an insulating layer 46 over the active region which inherently is the region including the channel and source and drain contact regions including junctions 20 underneath the gate 16 (cf. Figure 8 and col. 4, l. 46-57), an alloy layer of titanium alloy 40 (cf. col. 6, l. 34-47) within a contact opening in the insulating layer 46 (i.e., the "contact window" of conductor 48 through dielectric layer 46 (cf. col. 6, l. 66 – col. 7, l. 9) , the contact opening being at least partly over the active region (namely over source/drain regions with junctions 20) wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, *germanium*, lead, arsenic, and antimony, in particular: *germanium*; and a titanium silicide contact 38 (cf. col. 6, l. 34-47) having a composition different from the layer of titanium alloy (inherently the compositions of titanium silicide and titanium germanide are different), the contact being directly coupled to the layer (cf. Figure 7 and col. 6, l. 34-48; note that the titanium silicide is produced by an annealing step after the introduction of the germanium, and hence the silicide is in contact with the germanide).

The specific purpose of the teaching by Anjum et al is to reduce the required temperature for silicide formation and to reduce the thickness of the silicide layer, which if too thick would cause undue stresses in the layer (cf. col. 2, l. 25-42), in the formation of a barrier layer for the prevention of silicon migration into interconnect metal (cf. col. 1, l. 30-47). Said prevention is especially important for small-scale integrated circuits on a single chip (cf. col. 1, l. 13-30).

Motivation, to include the teaching by Anjun et al in the teaching by Nakamura et al is thus found in the objective by Nakamura on a memory device on a single chip (cf. col. 1, l. 5-10: integrated circuit) with increasingly fine element structures (cf. col. 2, l. 24-28) and the presence, in the invention by Nakamura et al of MOSFETs in all of the three cited components. The unspecified nature of the gate insulating film in the case of MISFETs as opposed to MOSFETs is irrelevant for this nexus. *Combination* of the teaching by Anjun et al in this regard and the invention by Nakamura et al is straightforward through the application to the source/drain contact structures in the MOSFETs by Nakamura et al of germanium to a titanium layer followed by annealing and removal of the upper portion of the titanium layer as disclosed by Anjun et al (cf. col. 6, l. 34-48), while the interconnect structure including conductive layer 48 extending through dielectric layer 46 thus teaching the contact hole as taught by Anjum et al is an obvious aspect of a MOSFET. *Success* in implementing said combination can therefore be reasonably expected.

On claim 63: the electronic device by Nakamura et al is a MOSFET (see above under claim 60) and hence includes a transistor (field effect transistor).

6. ***Claim 62*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al and Anjum et al as applied to claim 60 above, and further in view of Honeycutt et al (5,644,166). As detailed above, claim 60 is unpatentable over Nakamura et al in view of Anjum et al. Neither Nakamura et al nor Anjum et al necessarily teach the further limitation as defined by claim 62. However, it would have

been obvious to select an insulator layer that includes silicon dioxide in view of Honeycutt et al, who, in a patent on a contact structure to a semiconductor substrate (hence closely related to Anjum et al) teach the selection of a dielectric layer 16 that includes silicon dioxide (namely: BPSG; cf. col. 6, l. 60-65) for the purpose of allowing reflow at temperatures at or below 900 degrees of the contact hole to attain a relative high aspect ratio contact holes (cf. abstract). *Motivation*, to include the teaching by Honeycutt et al in this regard in the invention by Nakamura et al and Anjum et al, derives from the need for relatively high aspect ratio for contact holes due to decreased size of the openings of said contact holes (cf. Honeycutt et al, col. 1, l. 35-40) and the obvious increase of IC component density afforded by said decreased size. *Combination*, of said teaching with said invention, is straightforward through the selection of BPSG as the material for dielectric layer 46 in Anjum et al (Figure 8), which is the equivalent of dielectric layer 16 in Honeycutt et al.

7. ***Claim 64*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al in view of Anjum et al (5,4501,674) (cf. IDS of June 25, 2004).

Nakamura et al teach a memory (device) (cf. title, abstract and col. 1, l. 5-10) comprising: a semiconductor substrate (cf. abstract, first sentence, and col. 3, l. 66 – col. 4, l. 8); a memory array (cf. Figure 1 and col. 4, l. 8-35 and col. 13, l. 49-58) coupled to the semiconductor substrate (cf. abstract, first sentence, and col. 4, l. 66 – col. 7, l. 8); a control circuit (the word driver of Figure 8, col. 14, l. 66 – col. 15, l. 7 and col. 15, l.

59-67), operatively coupled to the memory array (the word driver inherently drives the gates of the memory array); an I/O circuit (input DIN / output buffer united into one input/output buffer) (cf. col. 8, l. 24-37), operatively coupled to the memory array (inherently so, because said input/output buffer belong to the peripheral circuits of the memory array and have the function to provide input and output functions for said memory array); a transistor (any of the MOSFETs in any of said memory array, control circuit or I/O circuit, inherently is a field effect transistor) (see col. 8, l. 53-58 for the MOSFETS in the memory array, col. 15, l. 59-67 for the MOSFETs in the control circuit, and Figure 9 and col. 15, l. 42-48 for the MOSFETs in the I/O circuit) formed on the semiconductor substrate (cf. abstract, first sentence and col. 3, l. 65 – col. 4, l. 8), the transistor having a source/drain region (inherent to any MOSFET) and an insulating layer over the source and drain region (inherent in any MOSFET is a gate insulating layer over the active region, which can be said to be also over said source/drain region as it has a higher altitude).

Nakamura et al do not necessarily teach the limitation that each of said MOSFETs to comprise the claimed alloy layer and titanium silicide contact as defined by claim 64.

However, it would have been obvious to include said limitation in view of Anjum et al: Anjum et al teach MISFET devices (cf. Figure 4, col. 5, l. 6-60) comprising: an insulating layer 46 over the active region which inherently is the region including the channel and source and drain contact regions including junctions 20 underneath the gate 16 (cf. Figure 8 and col. 4, l. 46-57) and which can be said to be also over the

source/drain region (superficial region within the semiconductor substrate with junction 20 (cf. col. 4, l. 45-57); an alloy layer of titanium alloy 40 (cf. col. 6, l. 34-47) within a contact opening in the insulating layer 46 (i.e., the "contact window" of conductor 48 through dielectric layer 46 (cf. col. 6, l. 66 – col. 7, l. 9) , the contact opening being at least partly over the source/drain region (namely over source/drain regions with junctions 20) wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, *germanium*, lead, arsenic, and antimony, in particular: *germanium*; and a titanium silicide contact 38 (cf. col. 6, l. 34-47) having a composition different from the layer of titanium alloy (inherently the compositions of titanium silicide and titanium germanide are different), the contact being directly coupled to the layer (cf. Figure 7 and col. 6, l. 34-48; note that the titanium silicide is produced by an annealing step after the introduction of the germanium, and hence the silicide is in contact with the germanide).

The specific purpose of the teaching by Anjum et al is to reduce the required temperature for silicide formation and to reduce the thickness of the silicide layer, which if too thick would cause undue stresses in the layer (cf. col. 2, l. 25-42), in the formation of a barrier layer for the prevention of silicon migration into interconnect metal (cf. col. 1, l. 30-47). Said prevention is especially important for small-scale integrated circuits on a single chip (cf. col. 1, l. 13-30).

Motivation, to include the teaching by Anjun et al in the teaching by Nakamura et al is thus found in the objective by Nakamura on a memory device on a single chip (cf. col. 1, l. 5-10: integrated circuit) with increasingly fine element structures (cf. col. 2, l.

24-28) and the presence, in the invention by Nakamura et al of MOSFETs in all of the three cited components. The unspecified nature of the gate insulating film in the case of MISFETs as opposed to MOSFETs is irrelevant for this nexus. *Combination* of the teaching by Anjun et al in this regard and the invention by Nakamura et al is straightforward through the application to the source/drain contact structures in the MOSFETs by Nakamura et al of germanium to a titanium layer followed by annealing and removal of the upper portion of the titanium layer as disclosed by Anjun et al (cf. col. 6, l. 34-48), while the interconnect structure including conductive layer 48 extending through dielectric layer 46 thus teaching the contact hole as taught by Anjum et al is an obvious aspect of a MOSFET. *Success* in implementing said combination can therefore be reasonably expected.

8. ***Claim 66*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al and Anjum et al as applied to claim 64 above, and further in view of Honeycutt et al (5,644,166). As detailed above, claim 64 is unpatentable over Nakamura et al in view of Anjum et al. Neither Nakamura et al nor Anjum et al necessarily teach the further limitation as defined by claim 66. However, it would have been obvious to select an insulator layer that includes silicon dioxide in view of Honeycutt et al, who, in a patent on a contact structure to a semiconductor substrate (hence closely related to Anjum et al) teach the selection of a dielectric layer 16 that includes silicon dioxide (namely: BPSG; cf. col. 6, l. 60-65) for the purpose of allowing reflow at temperatures at or below 900 degrees of the contact hole to attain a relative

high aspect ratio contact holes (cf. abstract). *Motivation*, to include the teaching by Honeycutt et al in this regard in the invention by Nakamura et al and Anjum et al, derives from the need for relatively high aspect ratio for contact holes due to decreased size of the openings of said contact holes (cf. Honeycutt et al, col. 1, l. 35-40) and the obvious increase of IC component density afforded by said decreased size. *Combination*, of said teaching with said invention, is straightforward through the selection of BPSG as the material for dielectric layer 46 in Anjum et al (Figure 8), which is the equivalent of dielectric layer 16 in Honeycutt et al.

9. ***Claim 67*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al and Anjum et al as applied to claim 64 above and further in view of Honeycutt et al (5,644,166). As detailed above, claim 64 is unpatentable over Nakamura et al in view of Anjum et al. Neither Nakamura et al not Anjum et al necessarily teach the further limitation as defined by claim 67. However, it would have been obvious to include said further limitation in view of Honeycutt et al, who, in a patent on a contact structure to a semiconductor substrate (hence closely related to Anjum et al) teach that by selecting the dielectric layer 16 (Honeycutt et al, col. 6, l. 55-65) to be made of BPSG (cf. col. 5, l. 3-4 and their claim 11) for enabling reflow at or below 900 degrees Celsius the attainment of high aspect ratio contact holes (cf. abstract; up to about 2:1). *Motivation*, to include the teaching by Honeycutt et al in this regard in the invention by Nakamura et al and Anjum et al, derives from the need for relatively high aspect ratio for contact holes due to decreased size of the openings of

said contact holes (cf. Honeycutt et al, col. 1, l. 35-40) and the obvious increase of IC component density afforded by said decreased size. *Combination*, of said teaching with said invention, is straightforward through the selection of BPSG as the material for dielectric layer 46 in Anjum et al (Figure 8), which is the equivalent of dielectric layer 16 in Honeycutt et al.

10. ***Claims 68, 70-72, 74-77 and 79-81*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al in view of Anjum et al (5,4501,674) and Honeycutt et al (5,644,166).

On claim 68: Nakamura et al teach a memory (device) (cf. title, abstract and col. 1, l. 5-10) comprising: a semiconductor substrate (cf. abstract, first sentence, and col. 3, l. 66 – col. 4, l. 8); a memory array (cf. Figure 1 and col. 4, l. 8-35 and col. 13, l. 49-58) coupled to the semiconductor substrate (cf. abstract, first sentence, and col. 4, l. 66 – col. 7, l. 8); a control circuit (the word driver of Figure 8, col. 14, l. 66 – col. 15, l. 7 and col. 15, l. 59-67), operatively coupled to the memory array (the word driver inherently drives the gates of the memory array); an I/O circuit (input DIN / output buffer united into one input/output buffer) (cf. col. 8, l. 24-37), operatively coupled to the memory array (inherently so, because said input/output buffer belong to the peripheral circuits of the memory array and have the function to provide input and output functions for said memory array); an electronic device (any of the MOSFETs in any of said memory array, control circuit or I/O circuit) (see col. 8, l. 53-58 for the MOSFETS in the memory array, col. 15, l. 59-67 for the MOSFETs in the control circuit, and Figure 9 and col. 15, l. 42-

48 for the MOSFETs in the I/O circuit) formed on the semiconductor substrate (inherent to a MOSFET is its coupling through a contact with a semiconductor substrate), the electronic device having an active region (inherent to any MOSFET).

Nakamura et al do not necessarily teach the limitation that each of said MOSFETs to comprise the claimed alloy layer and titanium silicide layer defined by claim 68.

However, it would have been obvious to include said limitation in view of Anjum et al: Anjum et al teach MISFET devices (cf. Figure 4, col. 5, l. 6-60) comprising: an insulating layer 46 over the active region which inherently is the region including the channel and source and drain contact regions including junctions 20 underneath the gate 16 (cf. Figure 8 and col. 4, l. 46-57), an alloy layer of titanium alloy 40 (cf. col. 6, l. 34-47) within a contact opening in the insulating layer 46 (i.e., the "contact window" of conductor 48 through dielectric layer 46 (cf. col. 6, l. 66 – col. 7, l. 9) , the contact opening being at least partly over the active region (namely over source/drain regions with junctions 20) wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, *germanium*, lead, arsenic, and antimony, in particular: *germanium*; and a titanium silicide contact 38 (cf. col. 6, l. 34-47) having a composition different from the layer of titanium alloy (inherently the compositions of titanium silicide and titanium germanide are different), the contact being directly coupled to the layer (cf. Figure 7 and col. 6, l. 34-48; note that the titanium silicide is produced by an annealing step after the introduction of the germanium, and hence the silicide is in contact with the germanide).

The specific purpose of the teaching by Anjum et al is to reduce the required temperature for silicide formation and to reduce the thickness of the silicide layer, which if too thick would cause undue stresses in the layer (cf. col. 2, l. 25-42), in the formation of a barrier layer for the prevention of silicon migration into interconnect metal (cf. col. 1, l. 30-47). Said prevention is especially important for small-scale integrated circuits on a single chip (cf. col. 1, l. 13-30).

Motivation, to include the teaching by Anjun et al in the teaching by Nakamura et al is thus found in the objective by Nakamura on a memory device on a single chip (cf. col. 1, l. 5-10: integrated circuit) with increasingly fine element structures (cf. col. 2, l. 24-28) and the presence, in the invention by Nakamura et al of MOSFETs in all of the three cited components. The unspecified nature of the gate insulating film in the case of MISFETs as opposed to MOSFETs is irrelevant for this nexus. *Combination* of the teaching by Anjun et al in this regard and the invention by Nakamura et al is straightforward through the application to the source/drain contact structures in the MOSFETs by Nakamura et al of germanium to a titanium layer followed by annealing and removal of the upper portion of the titanium layer as disclosed by Anjun et al (cf. col. 6, l. 34-48), while the interconnect structure including conductive layer 48 extending through dielectric layer 46 thus teaching the contact hole as taught by Anjum et al is an obvious aspect of a MOSFET. *Success* in implementing said combination can therefore be reasonably expected.

Neither Nakamura et al nor Anjum et al necessarily teach the further limitation of a borophosphosilicate glass (BPSG) layer over the active region. *However, it would*

have been obvious to include said further limitation in view of Honeycutt et al, who, in a patent on a contact structure to a semiconductor substrate (hence closely related to Anjum et al) teach that the dielectric layer 16 (Honeycutt et al, col. 6, l. 55-65) be made of BPSG (cf. col. 5, l. 3-4 and their claim 11) to enable reflow at or below 900 degrees Celsius to attain a relative high aspect ratio contact holes (cf. abstract). *Motivation*, to include the teaching by Honeycutt et al in this regard in the invention by Nakamura et al and Anjum et al, derives from the need for relatively high aspect ratio for contact holes due to decreased size of the openings of said contact holes (cf. Honeycutt et al, col. 1, l. 35-40) and the obvious increase of IC component density afforded by said decreased size. *Combination*, of said teaching with said invention, is straightforward through the selection of BPSG as the material for dielectric layer 46 in Anjum et al (Figure 8), which is the equivalent of dielectric layer 16 in Honeycutt et al.

On claim 70: the electronic device (MOSFET) includes a transistor (MAS field effect transistor).

On claim 71: the contact opening includes a high aspect ratio contact opening (cf. Honeycutt et al, abstract).

On claim 72: Nakamura et al teach a memory (device) (cf. title, abstract and col. 1, l. 5-10) comprising: a semiconductor substrate (cf. abstract, first sentence, and col. 3, l. 66 – col. 4, l. 8); a memory array (cf. Figure 1 and col. 4, l. 8-35 and col. 13, l. 49-58) coupled to the semiconductor substrate (cf. abstract, first sentence, and col. 4, l. 66 – col. 7, l. 8); a control circuit (the word driver of Figure 8, col. 14, l. 66 – col. 15, l. 7 and col. 15, l. 59-67), operatively coupled to the memory array (the word driver inherently

drives the gates of the memory array); an I/O circuit (input DIN / output buffer united into one input/output buffer) (cf. col. 8, l. 24-37), operatively coupled to the memory array (inherently so, because said input/output buffer belong to the peripheral circuits of the memory array and have the function to provide input and output functions for said memory array); an electronic device (any of the MOSFETs in any of said memory array, control circuit or I/O circuit) (see col. 8, l. 53-58 for the MOSFETS in the memory array, col. 15, l. 59-67 for the MOSFETs in the control circuit, and Figure 9 and col. 15, l. 42-48 for the MOSFETs in the I/O circuit) coupled to the semiconductor substrate (inherent to a MOSFET is its coupling through a contact with a semiconductor substrate), the electronic device having an active region (inherent to any MOSFET) as well as an insulator layer over the active region (inherent in MOSFET devices as well, because there should at least be the gate insulating layer and the interlayer dielectric over the active region).

Nakamura et al do not necessarily teach the limitation that each of said MOSFETs to comprise the claimed alloy layer and titanium silicide layer defined by claim 72.

However, it would have been obvious to include said limitation in view of Anjum et al and Honeycutt et al:

Anjum et al teach MISFET devices (cf. Figure 4, col. 5, l. 6-60) comprising: an alloy layer of titanium alloy 40 (cf. col. 6, l. 34-47) within a contact opening in the insulating layer 46 (i.e., the "contact window" of conductor 48 through dielectric layer 46 (cf. col. 6, l. 66 – col. 7, l. 9), the contact opening being at least partly over the active

region (namely over source/drain regions with junctions 20) wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, *germanium*, lead, arsenic, and antimony, in particular: *germanium*; and a titanium silicide contact 38 (cf. col. 6, l. 34-47) having a composition different from the layer of titanium alloy (inherently the compositions of titanium silicide and titanium germanide are different), the contact being directly coupled to the layer (cf. Figure 7 and col. 6, l. 34-48; note that the titanium silicide is produced by an annealing step after the introduction of the germanium, and hence the silicide is in contact with the germanide).

The specific purpose of the teaching by Anjum et al is to reduce the required temperature for silicide formation and to reduce the thickness of the silicide layer, which if too thick would cause undue stresses in the layer (cf. col. 2, l. 25-42), in the formation of a barrier layer for the prevention of silicon migration into interconnect metal (cf. col. 1, l. 30-47). Said prevention is especially important for small-scale integrated circuits on a single chip (cf. col. 1, l. 13-30).

Motivation, to include the teaching by Anjun et al in the teaching by Nakamura et al is thus found in the objective by Nakamura on a memory device on a single chip (cf. col. 1, l. 5-10: integrated circuit) with increasingly fine element structures (cf. col. 2, l. 24-28) and the presence, in the invention by Nakamura et al of MOSFETs in all of the three cited components. The unspecified nature of the gate insulating film in the case of MISFETs as opposed to MOSFETs is irrelevant for this nexus. *Combination* of the teaching by Anjun et al in this regard and the invention by Nakamura et al is

straightforward through the application to the source/drain contact structures in the MOSFETs by Nakamura et al of germanium to a titanium layer followed by annealing and removal of the upper portion of the titanium layer as disclosed by Anjun et al (cf. col. 6, l. 34-48), while the interconnect structure including conductive layer 48 extending through dielectric layer 46 thus teaching the contact hole as taught by Anjum et al is an obvious aspect of a MOSFET. *Success* in implementing said combination can therefore be reasonably expected.

Neither Nakamura et al nor Anjum et al necessarily teach the further limitation that said contact opening is a high aspect ratio contact opening. *However, it would have been obvious to include said further limitation in view of Honeycutt et al*, who, in a patent on a contact structure to a semiconductor substrate (hence closely related to Anjum et al) teach that the dielectric layer 16 (Honeycutt et al, col. 6, l. 55-65) be made of BPSG (cf. col. 5, l. 3-4 and their claim 11) to enable reflow at or below 900 degrees Celsius to attain a relatively high aspect ratio contact holes (cf. abstract). *Motivation*, to include the teaching by Honeycutt et al in this regard in the invention by Nakamura et al and Anjum et al, derives from the need for relatively high aspect ratio for contact holes due to decreased size of the openings of said contact holes (cf. Honeycutt et al, col. 1, l. 35-40) and the obvious increase of IC component density afforded by said decreased size. *Combination*, of said teaching with said invention, is straightforward through the selection of BPSG (cf. col. 9, l. 27-28) as the material for dielectric layer 46 in Anjum et al (Figure 8), which is the equivalent of dielectric layer 16 in Honeycutt et al, enabling high aspect ratio contact holes.

On claim 74: the electronic device, being a MOSFET is a field effect transistor, hence is a transistor.

On claims 75-76: the insulator layer in the combined invention, i.e., the dielectric layer 16 by Honeycutt et al, comprises silicon dioxide, if only because in one embodiment it is made of BPSG as explained above in the rejection of claim 72 (cf. col. 9, l. 27-28).

On claim 77: Nakamura et al teach a memory (device) (cf. title, abstract and col. 1, l. 5-10) comprising: a semiconductor substrate (cf. abstract, first sentence, and col. 3, l. 66 – col. 4, l. 8); a memory array (cf. Figure 1 and col. 4, l. 8-35 and col. 13, l. 49-58) coupled to the semiconductor substrate (cf. abstract, first sentence, and col. 4, l. 66 – col. 7, l. 8); a control circuit (the word driver of Figure 8, col. 14, l. 66 – col. 15, l. 7 and col. 15, l. 59-67), operatively coupled to the memory array (the word driver inherently drives the gates of the memory array); an I/O circuit (input DIN / output buffer united into one input/output buffer) (cf. col. 8, l. 24-37), operatively coupled to the memory array (inherently so, because said input/output buffer belong to the peripheral circuits of the memory array and have the function to provide input and output functions for said memory array); a transistor (any of the MOSFETs in any of said memory array, control circuit or I/O circuit) (see col. 8, l. 53-58 for the MOSFETS in the memory array, col. 15, l. 59-67 for the MOSFETs in the control circuit, and Figure 9 and col. 15, l. 42-48 for the MOSFETs in the I/O circuit) coupled to the semiconductor substrate (inherent to a MOSFET is its coupling through a contact with a semiconductor substrate), the transistor having a source/drain region (inherent to any MOSFET) as well as an

insulator layer over said source/drain region (inherent in MOSFET devices as well, because there should at least be the gate insulating layer and the interlayer dielectric over the active region).

Nakamura et al do not necessarily teach the limitation that each of said MOSFETs to comprise the claimed alloy layer and titanium silicide layer defined by claim 77.

However, it would have been obvious to include said limitation in view of Anjum et al and Honeycutt et al:

Anjum et al teach MISFET devices (cf. Figure 4, col. 5, l. 6-60) comprising: an alloy layer of titanium alloy 40 (cf. col. 6, l. 34-47) within a contact opening in the insulating layer 46 (i.e., the "contact window" of conductor 48 through dielectric layer 46 (cf. col. 6, l. 66 – col. 7, l. 9), the contact opening being at least partly over the source/drain region (namely over source/drain regions with junctions 20) wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, *germanium*, lead, arsenic, and antimony, in particular: *germanium*; and a titanium silicide contact 38 (cf. col. 6, l. 34-47) having a composition different from the layer of titanium alloy (inherently the compositions of titanium silicide and titanium germanide are different), the contact being directly coupled to the layer (cf. Figure 7 and col. 6, l. 34-48; note that the titanium silicide is produced by an annealing step after the introduction of the germanium, and hence the silicide is in contact with the germanide).

The specific purpose of the teaching by Anjum et al is to reduce the required temperature for silicide formation and to reduce the thickness of the silicide layer, which if too thick would cause undue stresses in the layer (cf. col. 2, l. 25-42), in the formation of a barrier layer for the prevention of silicon migration into interconnect metal (cf. col. 1, l. 30-47). Said prevention is especially important for small-scale integrated circuits on a single chip (cf. col. 1, l. 13-30).

Motivation, to include the teaching by Anjun et al in the teaching by Nakamura et al is thus found in the objective by Nakamura on a memory device on a single chip (cf. col. 1, l. 5-10: integrated circuit) with increasingly fine element structures (cf. col. 2, l. 24-28) and the presence, in the invention by Nakamura et al of MOSFETs in all of the three cited components. The unspecified nature of the gate insulating film in the case of MISFETs as opposed to MOSFETs is irrelevant for this nexus. *Combination* of the teaching by Anjun et al in this regard and the invention by Nakamura et al is straightforward through the application to the source/drain contact structures in the MOSFETs by Nakamura et al of germanium to a titanium layer followed by annealing and removal of the upper portion of the titanium layer as disclosed by Anjun et al (cf. col. 6, l. 34-48), while the interconnect structure including conductive layer 48 extending through dielectric layer 46 thus teaching the contact hole as taught by Anjum et al is an obvious aspect of a MOSFET. *Success* in implementing said combination can therefore be reasonably expected.

Neither Nakamura et al nor Anjum et al necessarily teach the further limitation that said contact opening is a high aspect ratio contact opening. *However, it would have*

been obvious to include said further limitation in view of Honeycutt et al, who, in a patent on a contact structure to a semiconductor substrate (hence closely related to Anjum et al) teach that the dielectric layer 16 (Honeycutt et al, col. 6, l. 55-65) be made of BPSG (cf. col. 5, l. 3-4 and their claim 11) to enable reflow at or below 900 degrees Celsius to attain a relatively high aspect ratio contact holes (cf. abstract). *Motivation*, to include the teaching by Honeycutt et al in this regard in the invention by Nakamura et al and Anjum et al, derives from the need for relatively high aspect ratio for contact holes due to decreased size of the openings of said contact holes (cf. Honeycutt et al, col. 1, l. 35-40) and the obvious increase of IC component density afforded by said decreased size. *Combination*, of said teaching with said invention, is straightforward through the selection of BPSG (cf. col. 9, l. 27-28) as the material for dielectric layer 46 in Anjum et al (Figure 8), which is the equivalent of dielectric layer 16 in Honeycutt et al, enabling high aspect ratio contact holes.

On claims 79-80: the insulator layer in the combined invention, i.e., the dielectric layer 16 by Honeycutt et al, comprises silicon dioxide, if only because in one embodiment it is made of BPSG as explained above in the rejection of claim 72 (cf. col. 9, l. 27-28).

On claim 81: Nakamura et al teach a memory (device) (cf. title, abstract and col. 1, l. 5-10) comprising: a semiconductor substrate (cf. abstract, first sentence, and col. 3, l. 66 – col. 4, l. 8); a memory array (cf. Figure 1 and col. 4, l. 8-35 and col. 13, l. 49-58) coupled to the semiconductor substrate (cf. abstract, first sentence, and col. 4, l. 66 – col. 7, l. 8); a control circuit (the word driver of Figure 8, col. 14, l. 66 – col. 15, l. 7 and

col. 15, l. 59-67), operatively coupled to the memory array (the word driver inherently drives the gates of the memory array); an I/O circuit (input DIN / output buffer united into one input/output buffer) (cf. col. 8, l. 24-37), operatively coupled to the memory array (inherently so, because said input/output buffer belong to the peripheral circuits of the memory array and have the function to provide input and output functions for said memory array); a transistor (any of the MOSFET transistors in any of said memory array, control circuit or I/O circuit) (see col. 8, l. 53-58 for the MOSFETS in the memory array, col. 15, l. 59-67 for the MOSFETs in the control circuit, and Figure 9 and col. 15, l. 42-48 for the MOSFETs in the I/O circuit) coupled to the semiconductor substrate (inherent to a MOSFET is its coupling through a contact with a semiconductor substrate), the transistor having a source/drain region (inherent to any MOSFET).

Nakamura et al do not necessarily teach the limitation that each of said MOSFETs to comprise the claimed alloy layer and titanium silicide layer defined by claim 81.

However, it would have been obvious to include said limitation in view of Anjum et al: Anjum et al teach MISFET devices (cf. Figure 4, col. 5, l. 6-60) comprising: an insulating layer 46 over the active region which inherently is the region including the channel and source and drain contact regions including junctions 20 underneath the gate 16 (cf. Figure 8 and col. 4, l. 46-57), an alloy layer of titanium alloy 40 (cf. col. 6, l. 34-47) within a contact opening in the insulating layer 46 (i.e., the "contact window" of conductor 48 through dielectric layer 46 (cf. col. 6, l. 66 – col. 7, l. 9) , the contact opening being at least partly over the active region (namely over source/drain regions

with junctions 20) wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, *germanium*, lead, arsenic, and antimony, in particular: *germanium*; and a titanium silicide contact 38 (cf. col. 6, l. 34-47) having a composition different from the layer of titanium alloy (inherently the compositions of titanium silicide and titanium germanide are different), the contact being directly coupled to the layer (cf. Figure 7 and col. 6, l. 34-48; note that the titanium silicide is produced by an annealing step after the introduction of the germanium, and hence the silicide is in contact with the germanide).

The specific purpose of the teaching by Anjum et al is to reduce the required temperature for silicide formation and to reduce the thickness of the silicide layer, which if too thick would cause undue stresses in the layer (cf. col. 2, l. 25-42), in the formation of a barrier layer for the prevention of silicon migration into interconnect metal (cf. col. 1, l. 30-47). Said prevention is especially important for small-scale integrated circuits on a single chip (cf. col. 1, l. 13-30).

Motivation, to include the teaching by Anjun et al in the teaching by Nakamura et al is thus found in the objective by Nakamura on a memory device on a single chip (cf. col. 1, l. 5-10: integrated circuit) with increasingly fine element structures (cf. col. 2, l. 24-28) and the presence, in the invention by Nakamura et al of MOSFETs in all of the three cited components. The unspecified nature of the gate insulating film in the case of MISFETs as opposed to MOSFETs is irrelevant for this nexus. *Combination* of the teaching by Anjun et al in this regard and the invention by Nakamura et al is straightforward through the application to the source/drain contact structures in the

MOSFETs by Nakamura et al of germanium to a titanium layer followed by annealing and removal of the upper portion of the titanium layer as disclosed by Anjun et al (cf. col. 6, l. 34-48), while the interconnect structure including conductive layer 48 extending through dielectric layer 46 thus teaching the contact hole as taught by Anjum et al is an obvious aspect of a MOSFET. *Success* in implementing said combination can therefore be reasonably expected.

Neither Nakamura et al nor Anjum et al necessarily teach the further limitation of a borophosphosilicate glass (BPSG) layer over the source/drain region. *However, it would have been obvious to include said further limitation in view of Honeycutt et al*, who, in a patent on a contact structure to a semiconductor substrate (hence closely related to Anjum et al) teach that the dielectric layer 16 (Honeycutt et al, col. 6, l. 55-65) be made of BPSG (cf. col. 5, l. 3-4 and their claim 11) to enable reflow at or below 900 degrees Celsius to attain a relative high aspect ratio contact holes (cf. abstract). *Motivation*, to include the teaching by Honeycutt et al in this regard in the invention by Nakamura et al and Anjum et al, derives from the need for relatively high aspect ratio for contact holes due to decreased size of the openings of said contact holes (cf. Honeycutt et al, col. 1, l. 35-40) and the obvious increase of IC component density afforded by said decreased size. *Combination*, of said teaching with said invention, is straightforward through the selection of BPSG as the material for dielectric layer 46 in Anjum et al (Figure 8), which is the equivalent of dielectric layer 16 in Honeycutt et al.

Allowable Subject Matter

11. ***Claims 83 and 84*** are allowed. The following is a statement of reasons for the indication of allowable subject matter: within the context of the invention as otherwise defined by claim 83 a titanium alloy layer overlying walls of a contact hole with a step coverage of more than 90% has not been found in the prior art.

Double Patenting

12. ***Claim 47*** is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6,433,434 in view of Anjum et al (5,401,674). Claim 2 in said patent claims:

"a memory comprising: a memory array comprising a layer of a titanium alloy comprising titanium and zinc, and a titanium silicide contact coupled to the layer" as does claim 47 of the invention (lines 1, 2 and 5-8 supplemented with the further limitation as defined by claim 47);

"a control circuit, operatively coupled to the memory array, the control circuit comprising a layer of a titanium alloy comprising titanium and zinc, and a titanium silicide contact coupled to the layer" as does claim 47 of the invention (lines 1, 3 and 5-8 supplemented with the further limitation as defined by claim 47);

"an I/O circuit, operatively coupled to the memory array, the I/O circuit comprising a layer of a titanium alloy comprising titanium and zinc, and a titanium silicide contact coupled to the layer" as does claim 47 of the invention (lines 1, 4 and 5-8 supplemented with the further limitation as defined by claim 47).

Said claim 2 of patent 6,433,434 does not claim the additional limitation contained within claim 47 of the invention that the coupling of the contact to the layer to be *direct*. However, it would have been obvious to include said additional limitation in view of Anjum et al, who, in a patent drawn to a contact structure over a silicide contact in a MISFET (hence art closely related to that of patent 6,433,434) teach said silicide contact to be *directly* coupled to the layer (cf. Figure 7, col. 6, l. 34-48 and col. 7, l. 6-9; note that the titanium silicide is produced by an annealing step *after* alloying the titanium, and hence the silicide is in contact with the titanium alloy layer). *Motivation*, to include the teaching in this regard by Anjum et al in the invention of patent 6,433,434, derives from the function of the titanium alloy layer as a barrier layer, to "maintain the silicon position during the anneal" (cf. Anjum et al, col. 3, l. 24-27). *Combination* of the teaching by Anjum et al with the invention of patent 6,533,434 is straightforwardly accomplished by alloying followed by an anneal step. *Success* in implementing the combination can therefore be reasonably expected.

13. ***Claim 47*** is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 46 and 47, respectively, of copending Application No. 09/940,917 (published as US 2002/0017724 A1) in view of Anjum et al (5,401,674).

This is a provisional obviousness-type double patenting rejection.

Claim 47 in said copending Application claims:

"a memory comprising: a memory array; a control circuit, operatively coupled to the memory array; an I/O circuit, operatively coupled to the memory array; and wherein

the memory array, control circuit and I/O circuit each comprise: a layer of titanium alloy, wherein the layer of titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and a titanium silicide contact" "coupled to the layer" (through the underlying independent claim 46, as does claim 46 of the invention underlying dependent claim 47 of the application (lines 1-9 supplemented with the further limitation as defined by claim 47) while claim 47 of the copending Application merely has the effect of selecting zinc of the said group, as also claimed in claim 47 of the invention; while the additional limitation that [the titanium silicide contact has] "a composition that is different from the layer of titanium alloy" is automatically satisfied by the selection of zinc.

The copending Application does not the claim limitation said coupling of the contact to the layer to be *direct*, in contrast with claim 47 through claim 46 of the invention. However, it would have been obvious to include said claim limitation in view of Anjum et al, who, in a patent drawn to a contact structure over a silicide contact in a MISFET (hence art closely related to that of copending Application 09/940,917) teach said silicide contact to be *directly* coupled to the layer (cf. Figure 7, col. 6, l. 34-48 and col. 7, l. 6-9; note that the titanium silicide is produced by an annealing step *after* alloying the titanium, and hence the silicide is in contact with the titanium alloy layer). *Motivation*, to include the teaching in this regard by Anjum et al in the invention of copending Application 09/940,917, derives from the function of the titanium alloy layer as a barrier layer, to "maintain the silicon position during the anneal" (cf. Anjum et al,

col. 3, l. 24-27). *Combination* of the teaching by Anjum et al with the invention of copending Application 09/940,917 is straightforwardly accomplished by alloying followed by an anneal step. *Success* in implementing the combination can therefore be reasonably expected.

Conclusion

14. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on June 25, 2004, prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
September 9, 2004